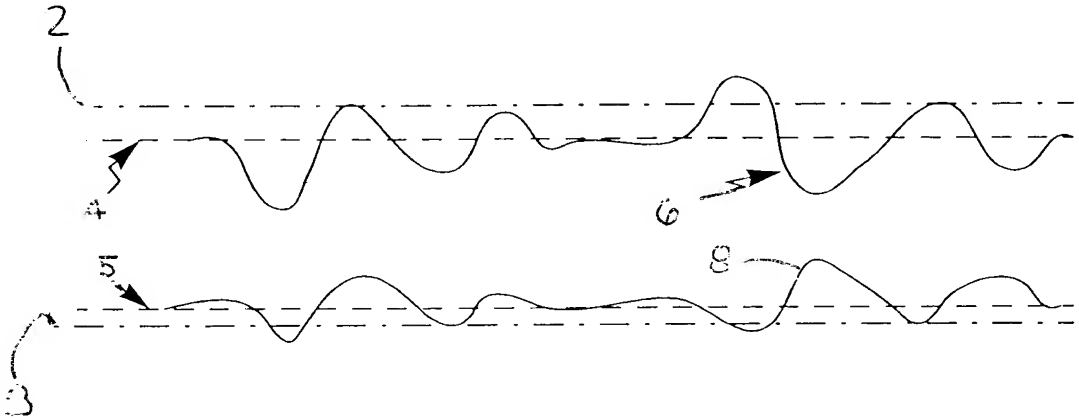

FIG 1

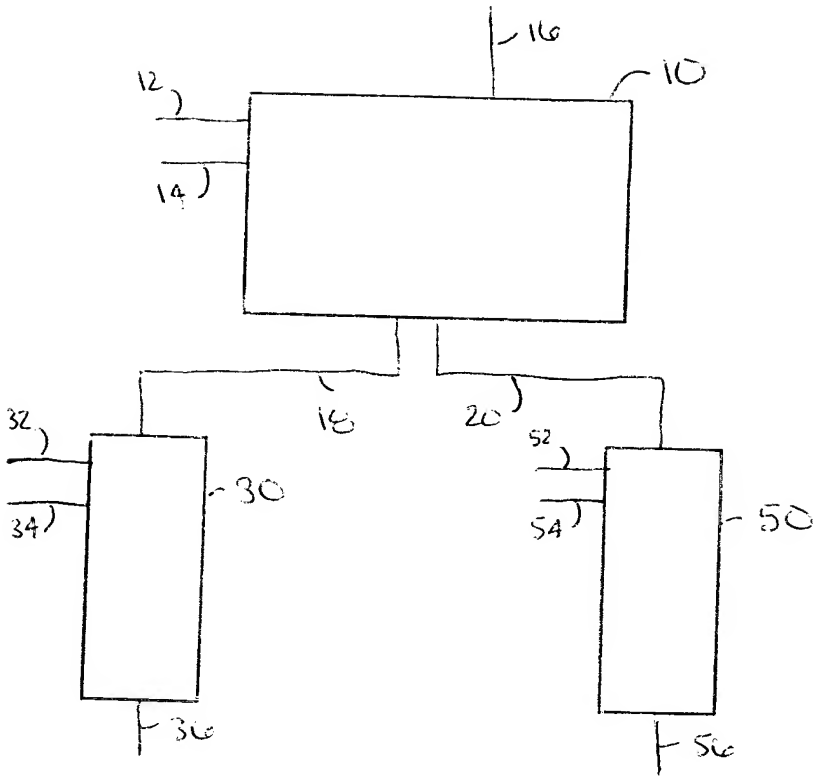

FIG. 2

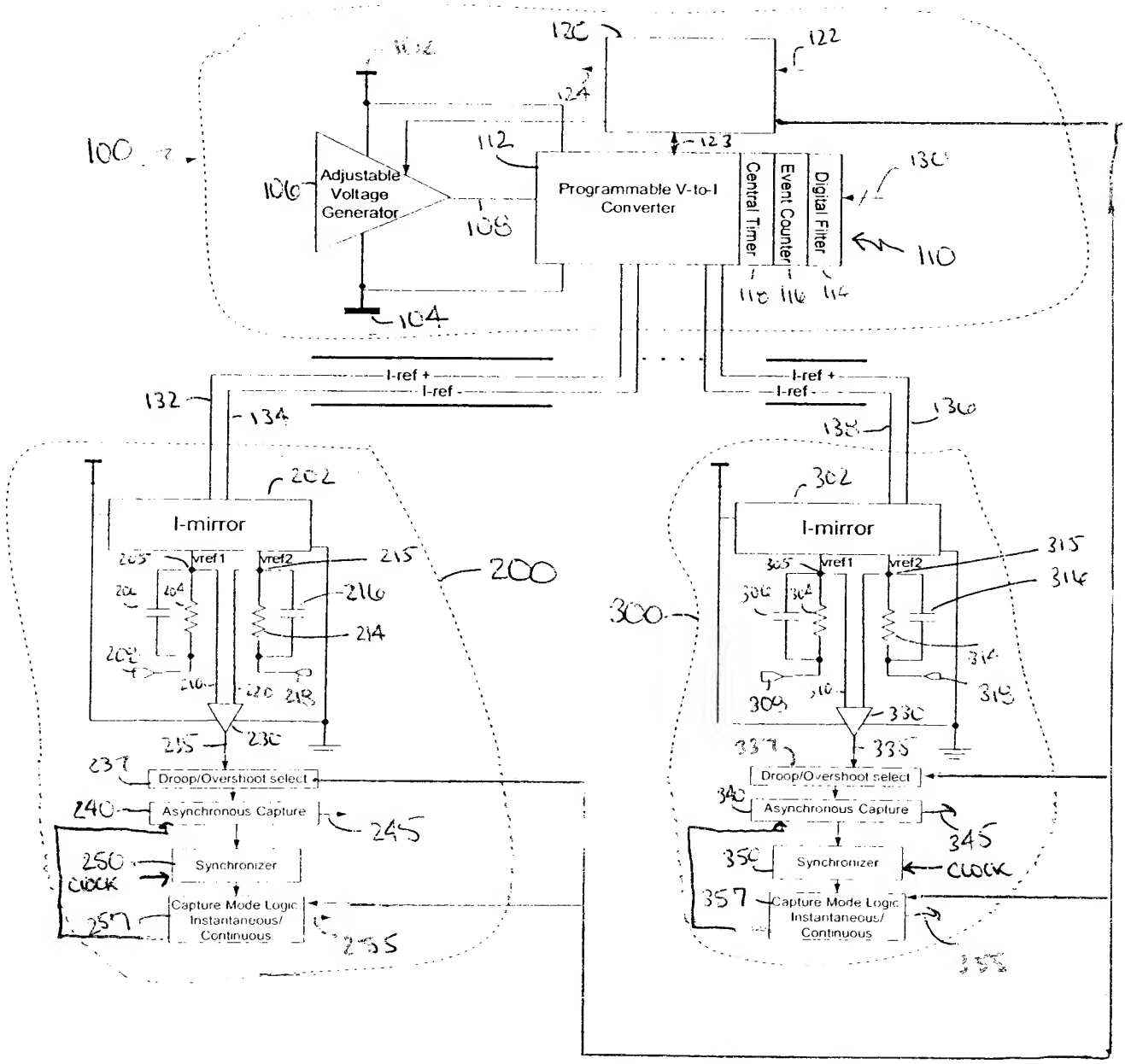
100
120
122
124
123
112
Adjustable Voltage Generator
106
108
Programmable V-to-I Converter
Central Timer
Event Counter
Digital Filter
130
110
104
I-ref +
I-ref -
132
134
136
138
I-mirror
202
200
300
302
vref1
vref2
215
216
214
220
218
230
235
237
Droop/Overshoot select
240
Asynchronous Capture
245
250
CLOCK
Synchronizer
257
Capture Mode Logic Instantaneous/ Continuous
255
315
316
314
310
330
335
340
345
350
357

FIG. 3

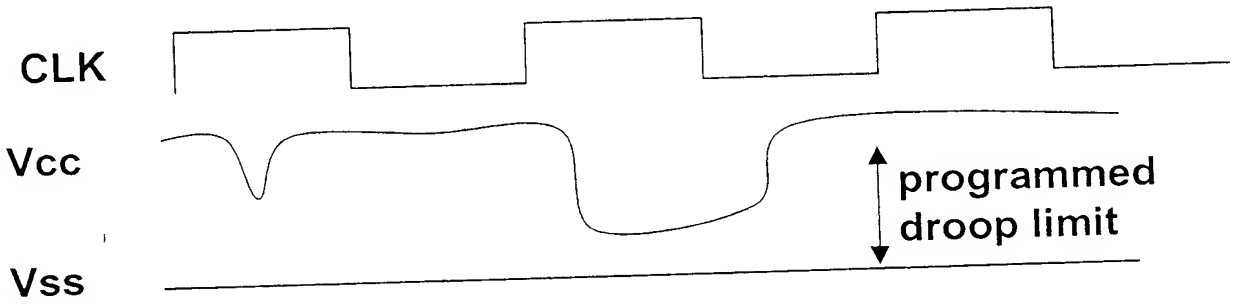

FIG. 4

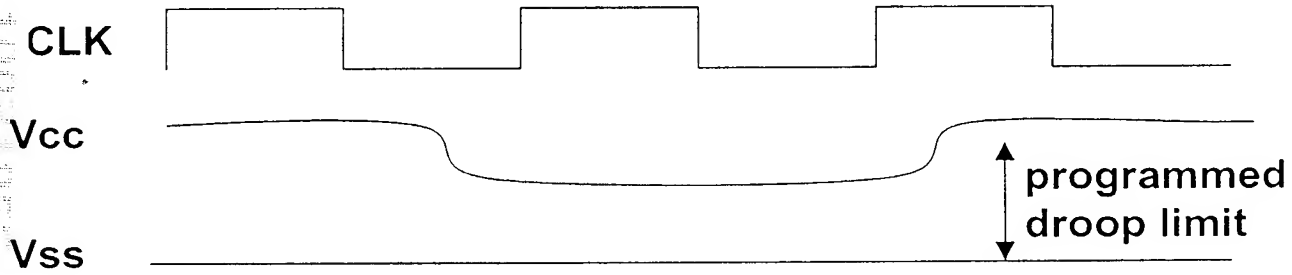

FIG. 5

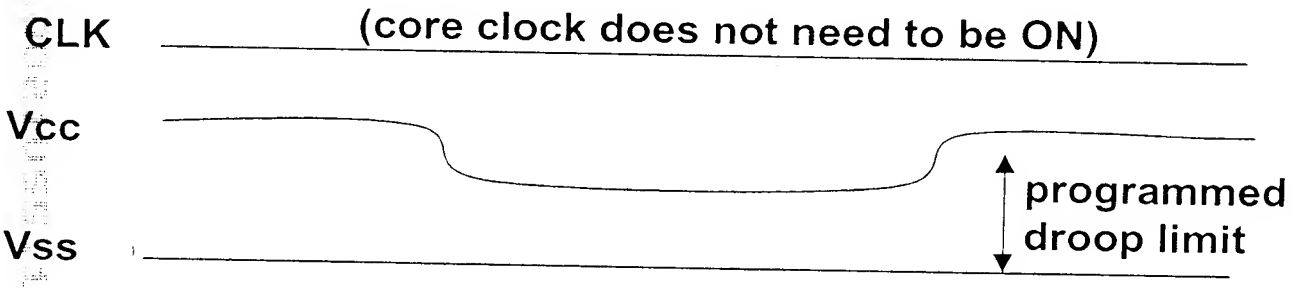
CLK
(core clock does not need to be ON)
Vcc
programmed
droop limit
Vss

FIG. 6

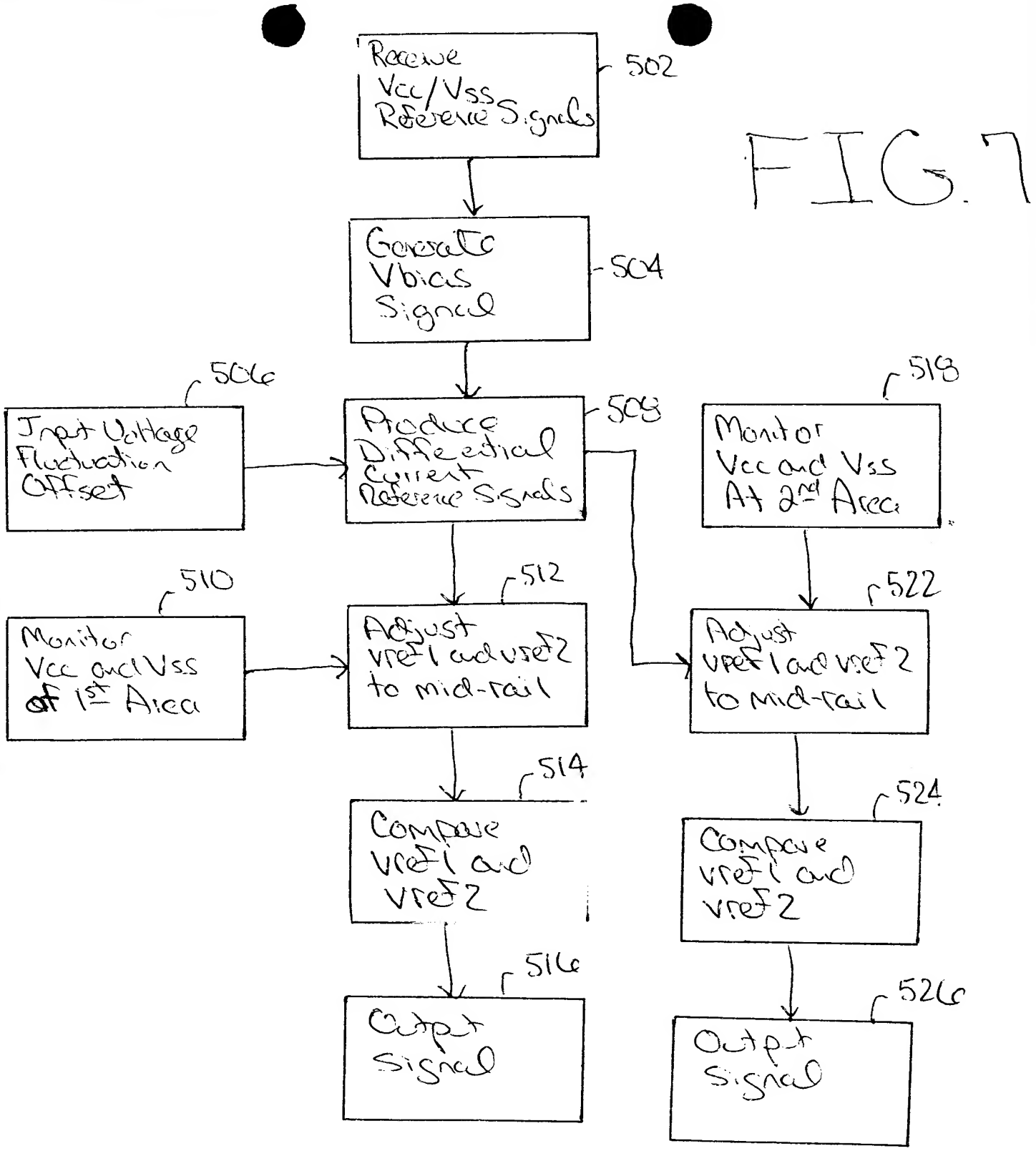
Receive Vcc/Vss Reference Signals
502
Generate Vbias Signal
504
Input Voltage Fluctuation Offset
506
Produce Differential Current Reference Signals
508
Monitor Vcc and Vss At 2nd Area
518
Monitor Vcc and Vss of 1st Area
510
Adjust vref1 and vref2 to mid-rail
512
Adjust vref1 and vref2 to mid-rail
522
Compare vref1 and vref2
514
Compare vref1 and vref2
524
Output Signal
516
Output Signal
526

FIG. 7

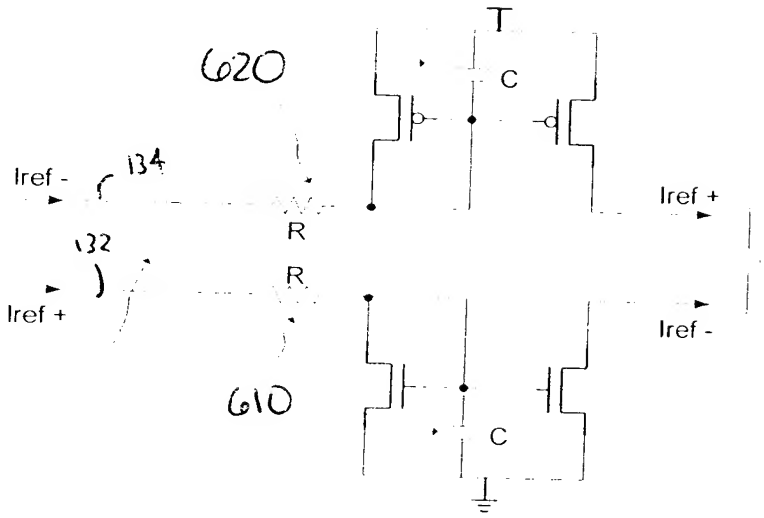

FIG 8